## REMARKS

Claims 1-36 were pending in the application. Claim 26 has been cancelled. Claims 1, 6-8, 10-12, 17-21, 27, 29, 30, 35, and 36 have been amended. Support for the amendments to claims 1, 6, and 21 may be found in the Specification on page 18, lines 7-26. Support for the amendments to claim 7 may be found in the Specification on page 18, line 19 – page 19, line 6. Support for the amendments to claims 8, 10-12, 17-20, 27, 29, 30, 35, and 36 may be found in the Specification on page 19, lines 7 – page 20, line 13. Accordingly, claims 1-25 and 27-36 are pending in the application.

### 35 U.S.C. § 103 REJECTIONS

In the Office Action of May 17, 2005, claims 1-36 stand rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 6,041,062 (hereinafter "Yamato"), in view of U.S. Patent 4,704,715 (hereinafter "Shibagaki"), in further view of U.S. Patent 6,055,242 (hereinafter "Doshi"), in further view of Applicant's admitted prior art. Applicant respectfully traverses these rejections and requests reconsideration in view of the following discussion.

Applicant submits that claim 1 as amended recites features which are neither disclosed nor suggested by the cited art. In paragraph 6 of the Office Action of May 17, 2005, the examiner states that Yamato discloses:

> "receiving a tributary (low-speed signal) (col. 4, lines 38-54 and col. 5, lines 6-13); recovering data from the tributary (col. 4, lines 38-54 and col. 5, lines 6-13); receiving a reference clock (clock supplier) (col. 4, lines 32-36; col. 5, lines 32-33; and col. 8, lines 48-56); generating at least two low-speed data channels (col. 4, lines 38-54 and col. 5, lines 6-13), where multiplexing STM-0 into high-order STM signals indicates two or more low-speed channels, wherein the low-speed data channels in aggregate contain the recovered data and each low-speed channel is timed by a clock based on the reference clock (col. 5, lines 32-33 and col.7, lines 15-34); and multiplexing the low-speed symbol channels to produce an electrical high-speed channel for transmission

in optical form across the communication system (Fig. 6; col. 7, lines 15-34; and col. 8, lines 15-23)."

However, claim 1, as amended, recites a method that includes:

"receiving a tributary complying with a jitter tolerance;
recovering data from the tributary;
receiving a reference clock;
**converting the recovered data into at least two intermediate-speed data channels, wherein each intermediate-speed data channel is timed by a first clock based on the reference clock;**
**converting each intermediate-speed data channel into at least two low-speed data channels,** wherein the low-speed data channels in aggregate contain the recovered data and each low-speed data channel is timed by a second clock based on the reference clock;
modulating each low-speed data channel to generate a corresponding low-speed symbol channel; and
frequency division multiplexing the low-speed symbol channels to produce an electrical high-speed channel for transmission in optical form across the communications system."

It is noted that the amendment includes the further limitation of converting the recovered data into at least two intermediate-speed data channels, wherein each intermediate-speed data channel is timed by a first clock based on the reference clock. The intermediate-speed data channels are then converted into at least two low-speed data channels. Further, at each conversion step, each channel is timed by a clock that is based on the reference clock. Neither the intermediate-speed data channels nor the timing of the intermediate-speed data channels by a first clock based on the reference clock are disclosed by the cited art.

More specifically, Yamato discloses:

"The first communication device receives data from the low-speed digital circuit, prepares serial data synchronized with the reference clock signal, and supplies the serial data and a frame signal to the second communication device. The second communication device prepares a high-speed synchronous multiplexed signal from the serial data and transmits the high-speed synchronous multiplexed signal to the high-speed synchronous multiplexing circuit.

> **The second communication device receives a high-speed synchronous multiplexed signal from the high-speed synchronous multiplexing circuit, prepares serial data synchronized with the reference signal from the high-speed synchronous multiplexed signal,** and transfers the serial data and a frame signal to the first communication device. The first communication device prepares a data signal from the serial data and transmits the data signal to the low-speed digital circuit." (Yamato, col. 4, lines 38-54).

Yamato also discloses:

> "The present invention also provides a high-speed synchronous multiplexing apparatus having a low-speed device and a high-speed device. The low-speed device converts a parallel STM-0 (or STS-1) signal and a serial STM-0 signal from one into another. **The high-speed device converts a serial STM-0 signal and a high-order STM signal from one into another.** The low- and high-speed devices are connected to each other through an electrical interface." (Yamato, col. 5, lines 6-13).

As highlighted in the first citation, Yamato discloses that the second communication device receives a high-speed synchronous multiplexed signal and prepares serial data synchronized with the reference signal from the high-speed synchronous multiplexed signal. This is further described by Yamato in the second citation in which the high-speed device is said to convert a high-order STM signal to a serial STM-0 signal. However, Yamato does not disclose converting a high-order STM signal to an intermediate-speed signal, timing an intermediate-speed signal by a first clock based on the reference clock or converting an intermediate-speed signal to at least two low-speed signals.

Neither does Applicant's admitted prior art (APA) disclose converting high-speed data channels into at least two intermediate-speed data channels, which are then converted into at least two low-speed data channels. Further, APA does not disclose that "each intermediate-speed data channel is timed by a first clock based on the reference clock", as recited in amended claim 1. Likewise, the features discussed above are wholly absent from Shibagaki and Doshi.

In summary regarding claim 1, Applicant finds no teaching or suggestion in the cited art, either singly or in combination, of converting the recovered data into at least two intermediate-speed data channels, wherein each intermediate-speed data channel is timed by a first clock based on the reference clock. Accordingly, Applicant submits that claim 1 is patentably distinguishable from the cited art for at least the above reasons. As independent claim 21 includes features similar to those of claim 1, claim 21 is believed patentably distinguishable from the cited art for similar reasons. Likewise, each of dependent claims 2-11, 22-25, and 27-29 are believed patentably distinguishable from the cited art for at least the above reasons as well.

Also, regarding claim 12, in paragraph 16 of the Office Action of May 17, 2005, the examiner states that Yamato discloses:

> "receiving an optical high-speed channel containing data transmitted across the communications system (col. 8, lines 24-34); demultiplexing an electrical high-speed channel, wherein the electrical high-speed channel is derived from the optical high-speed channel, into at least two low-speed symbol channels (col. 8, lines 24-34); recovering data from each low-speed data channel (col. 8, lines 24-34); generating a reference clock synchronized to the recovered data (col. 2, lines 24-47; col. 7, lines 15-34; and col 10, lines 33-40); and generating a tributary (transmitted low-speed signal), and the tributary is timed by a clock based on the reference clock (col. 2, lines 24-47; col. 7, lines 15-34; and col. 10, lines 33-40)."

However, claim 12 has been amended to recite features that are complimentary to those of claim 1. Specifically, claim 12 recites

> "receiving an optical high-speed channel containing data transmitted across the communications system, the data from a tributary complying with a jitter tolerance before said transmission;
> frequency division demultiplexing an electrical high-speed channel into at least two low-speed symbol channels, wherein the electrical high-speed channel is derived from the optical high-speed channel;
> demodulating each low-speed symbol channel to generate a corresponding low-speed data channel;
> recovering data from each low-speed data channel;
> generating a reference clock synchronized to the recovered data; and

**converting the low-speed data channels into at least two intermediate-speed data channels; and**

**converting the intermediate-speed data channels into a tributary**, wherein the tributary contains all of the recovered data, and the tributary is timed by a clock based on the reference clock and complies with the jitter tolerance."

It is noted that the amendment includes the further limitations of converting the low-speed data channels into at least two intermediate-speed data channels; and converting the intermediate-speed data channels into a tributary. As described below, Applicant submits that the cited art does not disclose these limitations.

More specifically, Yamato discloses:

> "The present invention also provides a high-speed synchronous multiplexing apparatus having a low-speed device and a high-speed device. The low-speed device converts a parallel STM-0 (or STS-1) signal and a serial STM-0 signal from one into another. **The high-speed device converts a serial STM-0 signal and a high-order STM signal from one into another.** The low- and high-speed devices are connected to each other through an electrical interface." (Yamato, col. 5, lines 6-13).

It is noted that Yamato discloses converting a serial STM-0 signal to a high-order STM signal. However, Yamato does not disclose converting the low-speed data channels into at least two intermediate-speed data channels; and converting the intermediate-speed data channels into a tributary. Neither does the remaining cited art disclose the above features.

In summary regarding claim 12, Applicant finds no teaching or suggestion in the cited art, either singly or in combination, of converting the low-speed data channels into at least two intermediate-speed data channels; and converting the intermediate-speed data channels into a tributary. Accordingly, Applicant submits that claim 12 is patentably distinguishable from the cited art for at least the above reasons. As independent claim 30 includes limitations similar to those of claim 12, claim 30 is believed patentably distinguishable from the cited art for similar reasons. Likewise, each of dependent claims 13-20 and 31-36 is believed patentably distinguishable from the cited art for at least the above reasons as well.

In addition to the above, Applicant submits the dependent claims recite additional features which are neither taught nor suggested by the cited art. For example, Applicant submits that claim 7, as amended, recites limitations neither taught nor suggested by the cited art. For example, claim 7 recites in part:

> "...converting each intermediate-speed data channel into at least two low-speed data channels comprises:
>
> dividing the phase-aligned reference clock to produce the first clock;
>
> retiming the recovered data in the intermediate-speed data channels using the first clock;
>
> time division demultiplexing the intermediate-speed data channels into the low-speed data channels."

It is noted that, as recited, a first clock is produced and used to retime the recovered data in the intermediate-speed data channels. Since the intermediate-speed data channels are wholly absent from the cited art, retiming the recovered data in the intermediate-speed data channels is also necessarily absent from the cited art, either singly or in combination. Accordingly, claim 7 is patentably distinguishable from the cited art for at least the above reasons.

In addition to the above, Applicant submits that claim 11, as amended, recites limitations neither taught nor suggested by the cited art. Claim 11, as amended, recites in part:

> "converting the receive-side intermediate-speed data channels into the tributary comprises:
>
> storing the recovered data from each receive-side intermediate-speed data channel;
>
> aligning a timing for the receive-side intermediate-speed data channels; and
>
> time division multiplexing the stored recovered data from the receive-side intermediate-speed data channels according to the aligned timing."

It is noted that the recovered data from each receive-side intermediate-speed data channel is stored and then time division multiplexed using aligned timing. Since the intermediate-speed data channels are wholly absent from the cited art, storing the intermediate-speed data channels and time division multiplexing them using aligned timing is also necessarily absent from the cited art, either singly or in combination. Accordingly, claim 11 is patentably distinguishable from the cited art for at least the above reasons. As claims 19, 29, and 36 include limitations similar to those of claim 11, claims 19, 29, and 36 are believed patentably distinguishable from the cited art for similar reasons.

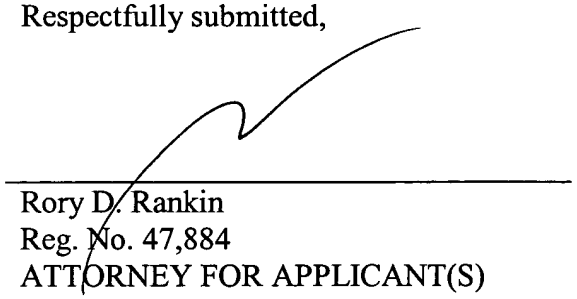
Applicant believes all claims to be in condition for allowance.

## CONCLUSION

Applicant submits the application is in condition for allowance, and an early notice to that effect is requested.

If any fees are due, the Commissioner is authorized to charge said fees to Meyertons, Hood, Kivlin, Kowert, & Goetzel, P.C. Deposit Account No. 501505/5957-41406/RDR.

Respectfully submitted,



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